WHAT IS CLAIMED IS:

1. A method of generating from a base clock signal having a predetermined frequency a baud clock signal for use in serial communications, comprising:

selecting a desired baud rate;

in response to the desired baud rate, providing a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval; and

dividing the base clock signal in response to said composite divisor to produce a baud clock signal which has a baud rate that approximates the desired baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses thereof and the extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

2. The method of Claim 1, including providing an oversampling factor indicative of a number of baud clock pulses within each symbol interval of the baud clock signal, said step of providing a composite divisor including providing the composite divisor in response to the oversampling factor and the desired baud rate.

3. The method of Claim 1, wherein the composite divisor includes a first divisor component indicative of the minimum time interval and a second divisor component which indicates that the leading edges of at least one pair of adjacent pulses are to be separated by the extended time interval.

4. The method of Claim 3, wherein said step of providing a composite divisor includes dividing the predetermined frequency of the base clock signal by the desired baud rate and by the oversampling factor to produce a quotient and a remainder, providing the quotient as the first divisor component, and providing the remainder as the second divisor component.

5. The method of Claim 4, wherein the remainder is modulo K, and K is the oversampling factor.

6. The method of Claim 3, wherein said step of providing a composite divisor includes providing a plurality of possible values of the first divisor component and providing for each of the possible values of the first divisor component a plurality of possible values of the second divisor component.

7. The method of Claim 6, including providing an oversampling factor indicative of a number of baud clock pulses within each symbol interval of the baud clock

signal, and producing the possible values of the second divisor component based on the oversampling factor.

8. The method of Claim 3, wherein said step of providing a composite divisor includes selecting from among a plurality of pairs of first and second divisor components one pair that will produce in said dividing step a baud clock signal having a baud rate that more closely approximates the desired baud rate than any other baud clock signal that could be produced in said dividing step using any of the remaining pairs of first and second divisor components.

9. The method of Claim 8, wherein said step of providing a composite divisor includes indexing the plurality of pairs of first and second divisor components against respective baud ranges.

10. The method of Claim 3, wherein said dividing step includes determining the minimum time interval and the extended time interval in response to the first divisor component and the predetermined frequency of the base clock signal, and selecting the at least one pair of adjacent pulses in response to the second divisor component.

11. The method of Claim 10, wherein said selecting step includes selecting in response to the second divisor component a plurality of pairs of adjacent pulses within each

symbol interval of the baud clock signal whose respective pairs of leading edges are to be separated by the extended time interval.

12. An apparatus for generating a baud clock signal for use in a serial communication interface, comprising:

a first input for receiving a base clock signal having a predetermined frequency;

a second input for receiving information indicative of a desired baud rate;

a divisor generator coupled to said second input for providing in response to the desired baud rate a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval; and

a clock divider coupled to said first input and said divisor generator and responsive to said composite divisor for dividing said base clock signal to produce a baud clock signal which has a baud rate that approximates the desired baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses thereof and the extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

13. The apparatus of Claim 12, wherein the composite divisor includes a first divisor component indicative of the minimum time interval and a second divisor component which indicates that the leading edges of at least one pair of adjacent pulses are to be separated by the extended time interval.

14. The apparatus of Claim 13, wherein said divisor generator includes a divider for dividing the predetermined frequency of the base clock signal by the desired baud rate and by an oversampling factor indicative of a number of baud clock pulses within each symbol interval of the baud clock signal to produce a quotient and a remainder, and wherein the quotient is the first divisor component and the remainder is the second divisor component.

15. The apparatus of Claim 14, wherein the remainder is a modulo K remainder, and wherein K is the oversampling factor.

16. The apparatus of Claim 13, wherein said divisor generator includes a look-up table having stored therein information indicative of a corresponding relationship between a plurality of baud rate ranges and respective pairs of said first and second divisor components.

17. The apparatus of Claim 13, wherein said clock divider includes a base clock counter responsive to said base clock and said first divisor component for determining said

minimum time interval and said extended time interval, a pulse generator coupled to said base clock counter for producing the baud clock signal in response to operation of said base clock counter, and a pulse position memory coupled to said base clock counter for storing information indicative of the at least one pair of adjacent pulses that are to be separated by the extended time interval.

18. The apparatus of Claim 17, wherein said pulse position memory includes an input for receiving said second divisor component, said pulse position memory responsive to said second divisor component for selecting said information indicative of the at least one pair of adjacent pulses.

19. The apparatus of Claim 18, wherein said pulse position memory includes a plurality of entries and is responsive to said second divisor component for selecting one of said entries, said clock divider including a baud clock counter coupled to said pulse generator for counting pulses of said baud clock signal, said baud clock counter having an output coupled to said pulse position memory, said pulse position memory responsive to said output of said baud clock counter for selecting a portion of said one entry.

20. The apparatus of Claim 12, wherein the serial communication interface is a UART.

21. A data processing apparatus capable of serial communication with an external device, comprising:

data processing circuitry for performing data processing operations on data involved in serial communication with the external device;

a serial communication interface coupled to said data processing circuitry for permitting serial communication between said data processing circuitry and the external device; and

a baud clock generator for generating a baud clock signal for use by the serial communication interface, said baud clock generator including a first input for receiving a base clock of the serial communication interface, said base clock having a predetermined frequency, a second input for receiving information indicative of a desired baud rate, a divisor generator coupled to said second input for providing in response to the desired baud rate a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval, and a clock divider coupled to said first input and said divisor generator and responsive to said composite divisor for dividing said base clock signal to

produce a baud clock signal which has a baud rate that approximates the desired baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses thereof and the extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

22. The apparatus of Claim 21, wherein said serial communication interface is a UART.

23. The apparatus of Claim 21, provided as one of a microprocessor, a digital signal processor, a modem, and a radiotelephone.

24. A data processing communication system, comprising:

a data processing apparatus and a device coupled externally to the data processing apparatus via a serial communication path;

said data processing apparatus including data processing circuitry for performing data processing operations on data involved in serial communication with said externally coupled device, a serial communication interface coupled between said data processing circuitry and said serial communication path for permitting serial communication between said data processing circuitry and the externally coupled device, and a baud clock generator for generating a baud clock signal for use by the serial communication interface; and

said baud clock generator including a first input for receiving a base clock of the serial communication interface, said base clock signal having a predetermined frequency, a second input for receiving information indicative of desired baud rate, a divisor generator coupled to said second input for providing in response to the desired baud rate a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval, and a clock divider coupled to said first input and said divisor generator and responsive to said composite divisor for dividing said base clock signal to produce a baud clock signal which has a baud rate that approximates the desired baud rate and which has within each symbol interval thereof at least said minimum time interval between the leading edges of all adjacent pulses thereof and said extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

25. The system of Claim 24, wherein said data processing apparatus is one of a microprocessor, a digital signal processor, a modem, a radiotelephone and a central processing unit of a laptop or desktop computer.

26. The system of Claim 25, wherein the externally coupled device is one of a microprocessor, a digital signal processor, a modem, a keyboard, a mouse, a printer and a laptop or desktop computer.

27. The system of Claim 24, wherein the externally coupled device is one of a microprocessor, a digital signal processor, a modem, a keyboard, a mouse, a printer and a laptop or desktop computer.

28. A method of generating from a base clock signal having a predetermined frequency a baud clock signal for use in receiving incoming data in serial communications, comprising:

receiving the incoming data at an unknown baud rate;

in response to the incoming data, providing a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval; and

dividing the base clock signal in response to said composite divisor to produce a baud clock signal which has the unknown baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses

thereof and the extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

29. The method of Claim 28, wherein said providing step includes providing the composite divisor in response to a start bit of the incoming data.

30. An apparatus for generating a baud clock signal for use in receiving incoming data in a serial communication interface, comprising:

a first input for receiving a base clock signal having a predetermined frequency;

a second input for receiving the incoming data at an unknown baud rate;

a divisor generator coupled to said second input for providing in response to the incoming data a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval; and

a clock divider coupled to said first input and said divisor generator and responsive to said composite divisor for dividing said base clock signal to produce a baud clock signal which has the unknown baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses thereof and the

extended time interval between the leading edges of at least one pair of adjacent pulses thereof.